



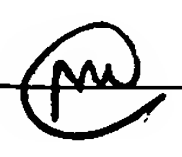
UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,215	09/09/2003	Francois Roy	S1022.81038US00	2710
23628	7590	10/12/2005	EXAMINER	
WOLF GREENFIELD & SACKS, PC FEDERAL RESERVE PLAZA 600 ATLANTIC AVENUE BOSTON, MA 02210-2211			NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/658,215	Applicant(s) ROY, FRANCOIS	
	Examiner Ori Nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 8-12 and 16-18 is/are rejected.
- 7) ☒ Claim(s) 5-7 and 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 8-11 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Merrill (5,614,744) or Chi et al. (5,587,596).

Regarding claims 1, 9, and 17, AAPA teaches in figures 1-4 and related text a monolithic photodetector comprising:

A pixel of a pixel matrix, said pixel further comprising:

a first active area (10) of doped single-crystal silicon corresponding to first (D2) and second (D3) photodiodes having a same surface area as two charge transfer MOS transistors (M4, M5), and as one storage diode (D1), a cathode of each photodiode being connected to a cathode of the storage diode via one of the charge transfer MOS transistors;

a second active area (18) of doped single-crystal silicon arranged next to a portion of the first active area (10) associated with the second photodiode (D3) and corresponding to a precharge switch having a first terminal connected to the cathode of

Art Unit: 2811

the storage diode (D1) and a second terminal connected to a reference voltage (33);
and

a third active (20) doped single-crystal silicon area arranged next to the portion of the first active area (10) associated with the first photodiode (D2) and corresponding to two read MOS transistors (M2, M3) in series, the gate (GM2, GM3) of one of the read transistors being connected to the cathode of the storage diode (D1) and the drain (DM2, DM3) or the source (SM2, SM3) of one of the read transistors (M2, M3) being connected to a processing system,

wherein the surfaces of the second and third active areas exposed to a lighting are substantially not identical.

AAPA does not teach second and third active areas in one pixel being substantially identical.

Merrill teaches in figure 5 and related text second and third active areas 16, 22 (source and drain regions) in one pixel being substantially identical.

Chi et al. teach in figure 3 and related text second and third active areas 116, 118 (source and drain regions) in one pixel being substantially identical.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use substantially identical second and third active areas (source and drain regions) in AAPA's device in order to simplify the processing steps of making the device and in order to obtain identical gain in two different active areas.

The combination is motivated by the teachings of AAPA who point out the disadvantages of using unidentical second and third active areas in one pixel.

Art Unit: 2811

Regarding claims 2 and 10, prior art's device comprises second and third active areas have substantially identical surface areas.

Regarding claims 3, 11 and 18, AAPA teaches first, second, and third active areas 10, 18, 20 are rectangular, the second and third active areas 18, 20 being of same dimensions and substantially aligned at a same distance from a side of the first active area 10.

Regarding claims 8 and 16, AAPA teaches the gates GM4, GM5 of the charge transfer MOS transistors M4, M5 correspond to portions of polysilicon strips 14, 16, which extend between the second and third active areas 18, 20.

Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), Merrill and Chi et al., as applied to claims 1 and 9 above, and further in view of Toyofuku (6,392,279).

AAPA, Merrill and Chi et al. teach substantially the entire claimed structure, as applied to claims 1 and 9 above, except a MOS transistor with two parallel gates. Toyofuku teaches in figures 1A-2C and related text MOS transistor with dual gates 7g. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Toyofuku into prior art's device in order to improve the short-channel effects and provide high current drive between two gates.

Art Unit: 2811

Allowable Subject Matter

Claims 5-7 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

The prior art of record does not teach or suggest, singularly or in combination at least the limitation the sum of the surface areas exposed to light of the third and fourth parallel polysilicon strips being substantially equal to the sum of the surface areas exposed to light of the first and second polysilicon strips.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 8-12 and 16-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2811

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

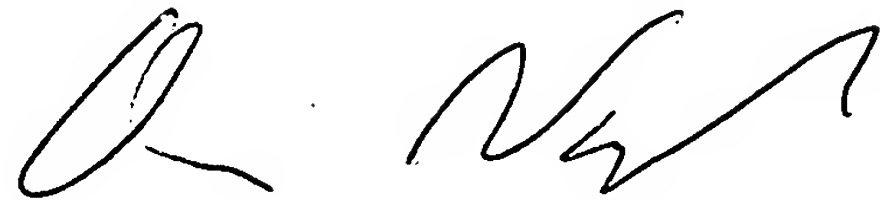
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Art Unit: 2811

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized, cursive script.

O.N.
10/8/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800